

Ashmit Singh

Electronics Engineering (VLSI) | VIT Vellore

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Education

Vellore Institute of Technology (VIT)

B.Tech in Electronics Engineering (VLSI Design and Technology); CGPA: 8.93/10.00

Vellore, Tamil Nadu, India

2024 – 2028

Springdales School, Dhaula Kuan

CBSE Board – Class XII: 93% — Class X: 89%

New Delhi, India

2024

Experience

🔗 Intern – Transportation (Automation & Infrastructure)

Delhivery Limited

May 2026 – Jul 2026

Gurugram, Haryana, India

- Architected an **8-node ROS2 DWS system** for a live warehouse line, replacing manual measurement at **~600 parcels/hour**.
- Built a 12-stage RealSense D455 perception stack (RANSAC, PCA boxes) at **±1 cm** over **100+** shipments.
- Designed a 16-state **FSM** gating vision on scale stability, cutting latency to **599 ms** (700 ms budget); sole developer.

🔗 Senior Robotic Arm Engineer, Team Vyadh (Martian Rover Team)

VIT Vellore

May 2025 – Present

Vellore, India

- Architected a **12 V/6 V power system** and **AS5600 encoder feedback loop** with tuned **PID** (sub-1°); **17th at IRC 2026**.
- Did **motor selection**, power calculations and hand-derived **FK/IK**; **3D-printed** motor mounts and a soil-scooping bucket.
- Developed a **ROS 2 Jazzy** stack (Jetson → **STM32 NUCLEO-F446ZE**), tested on the **NUCLEO-F446ZE**.

Projects

🔗 Harris Corner Detector ASIC – RTL to GDSII

SystemVerilog, Cadence Genus/Conformal/Tempus/Innovus, gscilib090 (90 nm)

- Designed a streaming Harris corner detector in SystemVerilog (**6-module pipeline**, **64-bit** response) at **1 pixel/clock**.
- Took it through the full **Cadence RTL-to-GDSII flow** in 90 nm: **250 MHz**, post-route setup WNS **+0.307 ns**, **54,154** cells, **127.3 mW**; DRC, connectivity and antenna checks all 0.
- Verified with **28 self-checking tests** across 5 image sizes plus 6 unit benches; **3,364 outputs**, **0 mismatches** against a bit-exact Python model; Conformal LEC **16,807** points equivalent, 0 non-equivalent.

🔗 Load-Aware Adaptive H-Bridge Motor Driver

Cadence Virtuoso, Spectre, gpd090 (90 nm CMOS)

- Designed at transistor level a brushed-DC driver whose **PWM duty falls as load current rises**, ahead of the hard trip; **8-instance** hierarchy of custom op-amp, comparator, Schmitt and RC-delay cells.
- **100 mΩ** shunt sensing with **~3.4 kHz** RC filter; RC dead-time (**~100 ns**) prevents shoot-through; overcurrent trip at **1.65 A**, UVLO and NOR SR fault latch.
- Spectre (1.8 V): duty fell **~85% → ~35%** as current rose **0.95 → 1.7 A**; fault asserted once in **~60 μs** and cleared.

🔗 Reliability-Aware Design-for-Test for Autonomous Robotic SoCs

SystemVerilog, Python, PODEM ATPG, MBIST, Yosys

- Built a runtime DFT architecture for a robotic SoC: **scan**, **PODEM ATPG interface**, **March C– MBIST**, online shadow test, fault injection and a scheduler ranking tests by criticality, health, aging and mission state.
- Fixed premature diagnostic-flag clearing with observability-aware evidence and rate-limited full-scan escalation: clears fell **117 → 0**; **2,267 of 2,440** flagged transients recovered in a **2,515-fault** campaign.
- Verified RTL against an independent Python model over **285,300 ticks × 55 signals**; **6/6** injected defects caught; **18/18** tests and **25** paper-claim checks passed.

Technical Skills

HDL & Verification: Verilog, SystemVerilog, RTL/FSM Design, Verilator, QuestaSim, Xcelium

EDA & Physical Design: Genus, Conformal LEC, Tempus, Innovus, Virtuoso, Spectre, Quartus, STA, CTS, DRC/LVS

Architecture & DFT: RISC-V, AXI4-Lite, DMA, Scan, ATPG (PODEM), MBIST, CMOS Analog/Digital Design

Robotics & Vision: ROS2, Kinematics, PID Control, OpenCV, MediaPipe, Open3D, Intel RealSense

Embedded: STM32, ESP32, Jetson Orin Nano, Arduino, UART, SPI, I2C, CAN, PWM

Languages & Tools: Python, C, C++, Perl, Tcl, MATLAB, Git, Linux, FastAPI, SQLite, Fusion 360